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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/810,284	03/26/2004	Robert J. Proebsting	SUN04-0110	9279

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EXAMINER	
LEVIN, NAUM B	

ART UNIT	PAPER NUMBER
2825	

DATE MAILED: 06/06/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/810,284	PROEBSTING ET AL.	
	Examiner	Art Unit	
	Naum B. Levin	2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 March 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-24* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *20* is/are allowed.

6)☒ Claim(s) *1-8, 12-16, 18-19, 21-24* is/are rejected.

7)☒ Claim(s) *9-11 and 17* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *26 March 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This office action is in response to application 10/810,284 filed on 03/26/2004. Claims 1-24 remain pending in the application.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1-2, 12-14, 21 and 23 are rejected under 35 U.S.C. 102(b) as being unpatentable by DeBrosse et al. (US Patent 5,534,732).

3. As to claims 1, 13, 21 and 23 DeBrosse discloses:

(1) An arrangement of differential pairs of wires that carry differential signals across a semiconductor chip, comprising:

a set of parallel tracks on the semiconductor chip that are used to route the differential pairs of wires ("integrated circuit layout of an interconnection array comprising a plurality of paired, parallel disposed line conductors" – col.1, ll.10-12) (col.1, ll.10-16; col.1, ll.51-67; col.2, ll.1-15);

wherein each differential pair of wires ("adjacent line conductors have now become differential noise sources" – col.4, ll.36-37) includes a true wire and a complement wire that carry corresponding true and complement signals ("The layout approach of the present invention is to separate on a planar surface the true and

complement lines of each pair of parallel line" – col.5, ll.20-22) (col.4, ll.33-51; col. 5, ll.20-28);

wherein the differential pairs of wires are non-adjacent, so that each true wire is separated from its corresponding complement wire by at least one intervening wire in the set of parallel tracks, thereby reducing coupling capacitance between corresponding true and complement wires ("The line conductors of each pair of line conductors of the plurality of paired line conductors are separated in the first region and in the second region such that capacitive coupling within each pair of line conductors is avoided" – col.2, ll.42-46) (col.2, ll.36-46; col.5, ll.20-41; col.6, ll.19-24; claim 13; Fig.5); and

one or more twisting structures, wherein a twisting structure twists a differential pair of wires so that the corresponding true and complement wires are interchanged within the set of parallel tracks ("The layout approach of the present invention is to separate on a planar surface the true and complement lines of each pair of parallel line ... A first region and a second region are defined on opposite sides of a crossing region disposed transverse the line conductors ... the crossing (or twisting) region is disposed intermediate the ends of the line conductors" – col.5, ll.20-28) (col.5, ll.20-28; col.6, ll.1-18; Figs. 5-11);

(13) A method for arranging differential pairs of wires to carry differential signals across a semiconductor chip, wherein each differential pair of wires includes a true wire and a complement wire that carry corresponding true

and complement signals, the method comprising (col.1, ll.10-12; col.4, ll.33-51; col. 5, ll.20-28):

defining a set of parallel tracks on the semiconductor chip, which are used to route the differential pairs of wires (col.1, ll.10-16; col.1, ll.51-67; col.2, ll.1-15);

mapping differential pairs of wires to tracks so that the differential pairs of wires are non-adjacent, which means that each true wire is separated from its corresponding complement wire by at least one intervening wire in the set of parallel tracks, thereby reducing coupling capacitance between corresponding true and complement wires (col.2, ll.36-46; col.5, ll.20-41; col.6, ll.19-24; claim 13; Fig.5); and

locating one or more twisting structures, wherein a twisting structure twists a differential pair of wires so that the corresponding true and complement wires are interchanged within the set of parallel tracks (col.5, ll.20-28; col.6, ll.1-18; Figs. 5-11);

(21) An arrangement of differential pairs of wires that carry differential signals across a semiconductor chip, comprising:

a set of parallel tracks on the semiconductor chip that are used to route the differential pairs of wires (col.1, ll.10-16; col.1, ll.51-67; col.2, ll.1-15);
wherein each differential pair of wires includes a true wire and a complement wire that carry corresponding true and complement signals) (col.4, ll.33-51; col. 5, ll.20-28); and

wherein the differential pairs of wires are non-adjacent, so that each true wire is separated from its corresponding complement wire by at least one intervening wire in

the set of parallel tracks, thereby reducing coupling capacitance between corresponding true and complement wires (col.2, ll.36-46; col.5, ll.20-41; col.6, ll.19-24; claim 13; Fig.5);

(23) A method for arranging differential pairs of wires to carry differential signals across a semiconductor chip, wherein each differential pair of wires includes a true wire and a complement wire that carry corresponding true and complement signals, the method comprising (col.1, ll.10-12; col.4, ll.33-51; col. 5, ll.20-28):

defining a set of parallel tracks on the semiconductor chip, which are used to route the differential pairs of wires (col.1, ll.10-16; col.1, ll.51-67; col.2, ll.1-15); and

mapping differential pairs of wires to tracks so that the differential pairs of wires are non-adjacent, which means that each true wire is separated from its corresponding complement wire by at least one intervening wire in the set of parallel tracks, thereby reducing coupling capacitance between corresponding true and complement wires (col.2, ll.36-46; col.5, ll.20-41; col.6, ll.19-24; claim 13; Fig.5).

4. As to claims 2, 12 and 14 DeBrosse recites:

(2), (14) The arrangement/method, wherein the one or more twisting structures are arranged so that substantially zero net differential coupling capacitance exists for each differential pair of wires (Abstract; col.1, ll.10-16);

(12) The arrangement, wherein the set of parallel tracks are located within the same metal layer in the semiconductor chip (col.10, ll.60-65).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 3-8, 15-16, 18-19, 22 and 24 are rejected under 35 U.S.C. 103(a) as being unpatentable by DeBrosse in view of Keeth (US Patent 6,043,562).

With respect to claims 3-8, 15-16, 18-19, 22 and 24 DeBrosse teaches the features above but lacks an arrangement/method of two differential pairs of wires/four adjacent tracks comprising three twisting/crossing structures (triple modified twist).

6. As to claims 18 and 19 Keeth recites:

(18) An arrangement of differential pairs of wires that carry differential signals across a semiconductor chip:

wherein the set of parallel tracks includes a possibly repeating pattern of four adjacent tracks, including a first track, which is adjacent to a second track, which is adjacent to a third track, which is adjacent to a fourth track (Fig. 13 - Triple Modified Twist);

wherein the differential pairs of wires include a first differential pair, A and A' , and a second differential pair, B and B' (see Appendix of Detailed Office Action);

wherein A starts in the first track, B starts in the second track, A' starts in the third track and B' starts in the fourth track (see section 1 of the Appendix in Detailed Office Action);

wherein a first twisting structure causes B and B' to interchange, so that A is in the first track, B' is in the second track, A' is in the third track and B is in the is in the fourth track (see section 2 of the Appendix in Detailed Office Action);

wherein a second twisting structure causes A and A' to interchange, so that A' is in the first track, B' is in the second track, A is in the third track and B is in the fourth track (see section 3 of the Appendix in Detailed Office Action); and

wherein a third twisting structure causes B' and B to interchange, so that A' is in the first track, B is in the second track, A is in the third track and B' is in the fourth track (see section 4 of the Appendix in Detailed Office Action);

(19) An arrangement of differential pairs of wires that carry differential signals across a semiconductor chip:

wherein the set of parallel tracks includes a possibly repeating pattern of four adjacent tracks, including a first track, which is adjacent to a second track, which is adjacent to a third track, which is adjacent to a fourth track (Single Modified Twist – Fig. 13);

wherein the differential pairs of wires include a first differential pair, A and A' , and a second differential pair, B and B' (Single Modified Twist – Fig. 13);

wherein A starts in the first track, B starts in the second track, A' starts in the third track and B' starts in the fourth track (Single Modified Twist – Fig. 13); and

wherein a first twisting structure causes A and A' to interchange, so that A' is in the first track, B is in the second track, A is in the third track and B' is in the fourth track (Single Modified Twist – Fig. 13).

It would have been obvious to a person of ordinary skills in the art at the time the invention was made to employ Keeth's teaching regarding the arrangement/method of two differential pairs of wires/four adjacent tracks comprising three twisting/crossing structures (triple modified twist) and use it in DeBrosse's invention by implementing more complex twisting schemes, thereby resolving the signal-to-noise problem that gets increasingly worse as semiconductor chip scale to smaller and smaller dimensions.

7. As to claims 3-8, 15-16, 22 and 24 Keeth discloses:

(3), (6), (15), (16), (22), (24) The arrangement/method, wherein the set of parallel tracks includes a possibly repeating pattern of four adjacent tracks, including a first track, which is adjacent to a second track, which is adjacent to a third track, which is adjacent to a fourth track (Fig. 13 - Triple Modified Twist);

wherein the differential pairs of wires include a first differential pair, A and A' , and a second differential pair, B and B' (see Appendix of Detailed Office Action);

wherein A starts in the first track, B starts in the second track, A' starts in the third track and B' starts in the fourth track (see section 1 of the Appendix in Detailed Office Action);

wherein a first twisting structure causes B and B' to interchange, so that A is in the first track, B' is in the second track, A' is in the third track and B is in the is in the fourth track (see section 2 of the Appendix in Detailed Office Action);

wherein a second twisting structure causes A and A' to interchange, so that A' is in the first track, B' is in the second track, A is in the third track and B is in the fourth track (see section 3 of the Appendix in Detailed Office Action); and

wherein a third twisting structure causes B' and B to interchange, so that A' is in the first track, B is in the second track, A is in the third track and B' is in the fourth track (see section 4 of the Appendix in Detailed Office Action);

(4), (5), (7), (8) The arrangement, wherein the first twisting structure is located approximately one quarter of the way down the set of parallel tracks (see the first twisting: between B and B' in the Appendix);

wherein the second twisting structure is located approximately one half of the way down the set of parallel tracks (see the second twisting: between A and A' in the Appendix); and

wherein the third twisting structure is located approximately three quarters of the way down the set of parallel tracks (see the third twisting: between B and B' in the Appendix).

Allowable Subject Matter

8. Claim 20 is allowed.

The following is a statement of reasons for the indication of allowable subject matter:

The prior art of record fails to teach or suggest or render obvious:

An arrangement of differential pairs of wires that carry differential signals across a semiconductor chip:

wherein the set of parallel tracks includes a possibly repeating pattern of six adjacent tracks, including a first track, which is adjacent to a second track, which is adjacent to a third track, which is adjacent to a fourth track, which is adjacent to a fifth track, which is adjacent to a sixth track;

wherein the differential pairs of wires include a first differential pair, A and A', a second differential pair, B and B', and a third differential pair, C and C';

wherein A starts in the first track, B starts in the second track, A' starts in the third track, C starts in the fourth track, B' starts in the fifth track and C' starts in the sixth track; and

wherein a first twisting structure causes A and A' to interchange, so that A' is in the first track, B is in the second track, A is in the third track, C is in the fourth track, B' is in the fifth track and C' is in the sixth track.

9. Claims 9-11 and 17 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is a statement of reasons for the indication of allowable subject matter:

The prior art of record fails to teach or suggest or render obvious:

An arrangement/method of differential pairs of wires that carry differential signals across a semiconductor chip, comprising:

a set of parallel tracks on the semiconductor chip that are used to route the differential pairs of wires;

wherein each differential pair of wires includes a true wire and a complement wire that carry corresponding true and complement signals;

wherein the differential pairs of wires are non-adjacent, so that each true wire is separated from its corresponding complement wire by at least one intervening wire in the set of parallel tracks, thereby reducing coupling capacitance between corresponding true and complement wires;

wherein one or more twisting structures, wherein a twisting structure twists a differential pair of wires so that the corresponding true and complement wires are interchanged within the set of parallel tracks;

wherein the one or more twisting structures are arranged so that substantially zero net differential coupling capacitance exists for each differential pair of wires;

wherein the set of parallel tracks includes a possibly repeating pattern of six adjacent tracks, including a first track, which is adjacent to a second track, which is adjacent to a third track, which is adjacent to a fourth track, which is adjacent to a fifth track, which is adjacent to a sixth track;

wherein the differential pairs of wires include a first differential pair, A and A', a second differential pair, B and B', and a third differential pair, C and C';

wherein A starts in the first track, B starts in the second track, A' starts in the third track, C starts in the fourth track, B' starts in the fifth track and C' starts in the sixth track; and

wherein a first twisting structure causes A and A' to interchange, so that A' is in the first track, B is in the second track, A is in the third track, C is in the fourth track, B' is in the fifth track and C' is in the sixth track.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Naum B. Levin whose telephone number is 571-272-1898. The examiner can normally be reached on M-F (8:00-4:30).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jack Chiang can be reached on 571-272-7483. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Uuando
THUAN DO
Primary examiner.
5/24/06.

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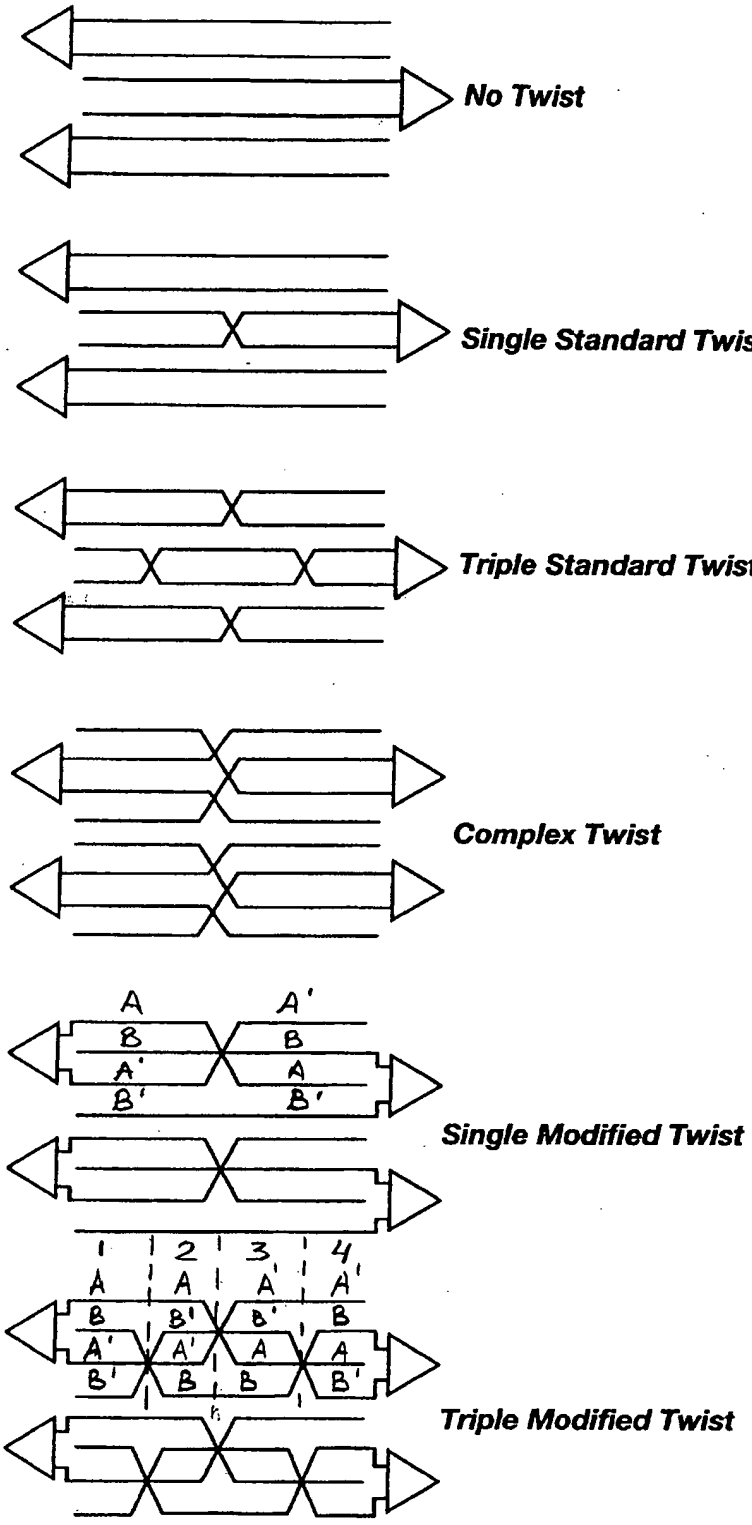
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Fig. 13